IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method comprising:

determining whether a virtual address is stored in a translation lookaside buffer (TLB), the TLB including a plurality of entries, wherein the entries include a minimum virtual page ~~number~~ size bit string and a variable bit string, the determining including,

comparing a first bit string of the virtual address to the minimum virtual page ~~number~~ size bit string of each of the entries;

determining whether the first bit string matches the minimum virtual page ~~number~~ size bit string of one of the entries;

if the first bit string matches the minimum virtual page number bit string of one of the entries, decoding a page size stored in the variable ~~portion~~ bit string of the matching entry and a ~~1 bit~~ data field associated with the matching entry, wherein the decoding determines a set of bits ~~of~~ in the variable bit string; and

comparing the set of bits of the variable ~~portion~~ bit string of the matching entry to a second bit string of the virtual address.

2. (Original) The method of claim 1 further comprising:

if the set of bits matches the second bit string, generating a hit indication; and

if the set of bits does not match the second bit string, generating a miss indication.

3. (Original) The method of claim 1, where the TLB is a fully associative TLB.

4. (Original) The method of claim 1, wherein a page size is encoded in the second bit string.

5. (Original) The method of claim 1, wherein the TLB is a first level TLB.

6. (Original) A method comprising:

determining a page size encoded in a virtual address tag, wherein the virtual address tag is stored in a translation lookaside buffer entry, and wherein the virtual address tag includes a set of bits, wherein each bit of the set indicates whether an additional bit is needed to represent the page size, the determining including,

inspecting a first bit stored in a 1-bit field of the TLB;

determining whether the first bit indicates that at least another bit is needed to represent the page size;

if at least another bit is needed to represent the page size, repeatedly inspecting successive bits of the set until a bit of the set indicates that an additional bit is not needed to represent the page size, and determining the page size based on the number of bits inspected.

7. (Original) The method of claim 6, wherein the TLB is a fully associative TLB.

8. (Original) The method of claim 6, wherein the page size ranges from 4Kb to 4Tb.

9. (Original) The method of claim 6, wherein the TLB is a first level TLB.

10. (Original) The method of claim 6, wherein the page size is represented a 4-bit string.

11. (Currently Amended) An apparatus comprising:

a translation lookaside buffer (TLB) to receive a virtual address, wherein the TLB includes a plurality of entries, wherein each of the plurality of entries includes a minimum virtual page ~~number~~ size bit string, a variable bit string, and a 1-bit field, the translation lookaside buffer including,

a first set of comparators to compare a first bit string of the virtual address to the minimum virtual page ~~number~~ size bit string of each of the plurality of entries;

a second set of decoder-comparators to decode a page size encoded in the variable bit string and the ~~1-bit~~ data field of each entry, and to compare a portion of

the variable bit string to a second bit string of the virtual address, wherein the portion is based on the page size.

12. (Currently Amended) The apparatus of claim 11 further comprising:
a page mask register to provide ~~the~~ a current page size;
a hit logic unit coupled to the page mask register, the first set of comparators, and the second set of decoder-comparators, the hit logic to determine whether the current page size is less than or equal to the page size.

13. (Currently Amended) The apparatus of claim 11, wherein the hit logic generates a miss indication after determining that ~~the~~ a current page size is less than ~~or equal to~~ the page size.

14. (Original) The apparatus of claim 11, wherein the TLB is a fully associative TLB.

15. (Original) The apparatus of claim 11, wherein the TLB is a first level TLB.

16. (Original) An apparatus comprising:
a translation lookaside buffer (TLB) including a plurality of entries, wherein each of the entries includes,
a virtual address tag field;
a variable bit string to store an encoded page size;
a 1-bit field to store information used in decoding the encoded page size; and
a page frame number field;
the TLB also including,
a set of decoder-comparators, wherein one of the set of decoder-comparators is associated with each of the entries, and wherein the decoder-comparators decode the encoded page size stored in the variable bit string, and wherein the decoder-comparators compare a part of the variable bit string with a part of a virtual page number.

17. (Original) The apparatus of claim 16, wherein the TLB is fully associative.

18. (Original) The apparatus of claim 16, wherein the TLB is a fist level TLB.

19. (Original) The apparatus of claim 16 further comprising:

a page mask register to provide a current page size;

a hit logic unit coupled to the TLB and the page mask register, the hit logic unit to determine whether the current page size is less than or equal to the decoded page size.

20. (Currently Amended) The apparatus of claim 16, wherein the hit logic generates a miss indication after determining ~~the~~ a current page size is less than ~~or equal to~~ the decoded page size.